MICROPROGRAMMABLE INTEGRATED DATA ACQUISITION SYSTEM-FATIGUE LIFE DATA APPLICATION

Wesley Craig Stanfield

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THESIS

MICROPROGRAMMABLE INTEGRATED DATA ACQUISITION SYSTEM-FATIGUE LIFE DATA APPLICATION

by

Wesley Craig Stanfield

March 1976

Thesis Advisor: G. H. Lindsey

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The "Microprogrammable Integrated Data Acquisition System-Fatigue Life Data Application" (Midas FLD) is a microprocessor based data acquisition system. It incorporates a Pro-Log Corporation MPS 803 microprocessor, Microvox wafer recorder and various integrated circuit devices to process analog signals. The program written for the MPS 803 is dedicated to processing and recording in sequence aircraft fatigue data originating from

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strain gages located at fatigue critical points. This thesis describes the various modules of the system and details the development process used in constructing Midas FLD, including the application of the PL/M compiler, Intellec 8 development computer and associated testers. Appendix II gives detailed instructions for reconstructing Midas FLD.

Microprogrammable Integrated Data Acquisition System-Fatigue Life Data Application

by

Wesley Craig Stanfield

Lieutenant, United States Navy

B.S., United States Naval Academy, 1969

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ABSTRACT

The "Microprogrammable Integrated Data Acquisition System-Fatigue Life Data Application" (Midas FLD) is a microprocessor based data acquisition system. It incorporates a Pro-Log Corporation MPS 803 microprocessor, Microvox wafer recorder and various integrated circuit devices to process analog signals. The program written for the MPS 803 is dedicated to processing and recording in sequence aircraft fatigue data originating from strain gages located at fatigue critical points. This thesis describes the various modules of the system and details the development process used in constructing Midas FLD, including the application of the PLM compiler, Intellec 8 development computer and associated testers. Appendix II gives detailed instructions for reconstructing Midas FLD.

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I. INTRODUCTION

The considerations justifying the need for the Microprogrammable Integrated Data Acquisition System-Fatigue Life Data Application (Midas FLD) have been set forth by Lcdr. D. M. Vidrine in his thesis "A Sequential Strain Monitor and Recorder for Use in aircraft Fatigue Life Prediction" [Vidrine, 1975]. They include: 1) the critical nature of weight minimization in aircraft design and the opposing desire to utilize aircraft to the maximum of their fatigue life without sacrificing safety; 2) the inherent human errors in the data processing and the associated need for numerous verifications of data; and 3) the failure of the counters to record sequential information.

Lcdr. Vidrine, with assistance from Lt. James W. Sturges, successfully applied the Midas general system [Sturges, 1975] to the fatigue life data monitoring problem and proved its usefulness; however, the space limitations of high performance aircraft dictate that the next consideration be the modification of the general system to fit the space restrictions. This thesis describes the modified system which is designated Midas FLD.

II. OVERALL SYSTEM DESCRIPTION

Midas FLD functions in the same manner as Lcdr. Vidrine's "Sequential Strain Monitor" (SSM). The major differences are that in processing analog signals, Midas FLD is limited to eight signals. Midas FLD utilizes less expensive components to perform the multiplexer and analog-to-digital conversion functions than the commercially obtained Datel DAS 16 used in SSM. In place of the larger MPS 805 microprocessor, an MPS 803 is used for signal filtering. The recording device is a Micro Communications Corp. Microvox recorder, replacing the larger, more expensive, although greater capacity, Memodyne tape recorder. Smaller tape wafers are used in place of cassette tapes having a capacity of storing 5,200 strain significant vectors of eight elements each or a total of 41,600 strain significant events, about one-eighth the capacity of the cassettes.

The most significant difference is the development process used to generate the Midas FLD system computer program. SSM was developed entirely from machine code language and programmed machine code step by machine code step with the Pro-Log Corporation "Suitcase Programmer." In contrast, Midas FLD utilizes the PLM compiler [Intel, 1975] resident on the Naval Postgraduate School's IBM 360 computer to produce the machine code program from a high level PLM program. This machine code program in paper tape form is then read into an Intel 8008 development microcomputer, which programs the Midas FLD "programmable read-only memories" (PROM's) at a rate of approximately 256 machine code steps every 20 seconds. The advantages of the development system will be clearly demonstrated when the Midas FLD software is discussed later.

Attention is now turned to the design and description

of the individual components of the Midas FLD system.

A. MPS 803 MICROPROCESSOR

The Midas FLD system is built around the MPS 803 microprocessor, and all other considerations stem from the specifications of the MPS 803. These specifications are given in "The Designer's Guide to Programmed Logic for MPS 800 Systems" [Biewer, 1974], and those essential to the design of the system are:

1. Input-Output Capacity

The MPS 803 has a capacity of 28 separate lines selectable as input or output signal lines. Designation of lines as either input or output is accomplished through a simple hardware adjustment. The fact that there are only 28 lines available limits the number of peripheral devices the MPS 803 can control.

These lines are TTL compatable, which means they can be used to interface with components whose signal levels correspond to "Transistor to Transistor Logic" levels. This governs the choice of peripheral devices.

2. Memory Capacity

The "Read Only Memory" (PROM) capacity of the MPS 803 microprocessor is 1024 machine code words, 256 words on each of four PROMs. Since the control program is stored on PROMs, the complexity of the data filtering is limited by this capacity.

It is noted that this is a severe limitation, and due consideration of the size of the control program prior to obtaining the microprocessor is mandatory.

3. Central Processing Unit (CPU)

The MPS 803 utilizes an Intel 8008 CPU, which dictates the instruction set to be used.

a. Instruction Set

More advanced CPUs, such as the Intel 8080, incorporate a higher level instruction set and can thus perform more complex operations on data with fewer instructions than the earlier 8008 CPU. Since the 8008 development system was the only one available at the time of design, Midas FLD is designed around the more restrictive 8008 CPU.

b. Time State

Midas FLD uses an 8008 CPU with a time state of 2.8 microseconds; i.e., the reference time unit for determining how long it takes the CPU to perform an operation is 2.8 microseconds. Table 1 shows the comparison of execution times for the 2.8 and 4.0 microsecond time state machines.

Accurate timing delays may be necessary in order to synchronize MPS 803 signals to timed events (such as data clocks). An alternative to this synchronization is to monitor the external timing device (such as the clock pulse produced by the microrecorder) for these events. Midas FLD uses the monitoring technique (see "BIT$RECORD" procedure in part IV.), thus bypassing the need for accurate time computation. The time state consideration enters in the 20 second landing roll-out provision (see "DELAY" part IV.).

	NUMBER OF INSTRUCTION WORDS	INSTRUCTION CATEGORY			NUMBER OF TIME STATES	EXECUTION TIME 4.0 μ SEC. T STATE	EXECUTION TIME 2.8 μ SEC. T STATE
REGISTER	1	LRR	LOAD REGISTER WITH REGISTER		5	20	14.0
	2	LRI	LOAD REGISTER IMMEDIATE		8	32	22.4
	1	CNT	COUNT REGISTER		5	20	14.0
MEMORY	1	LRM	LOAD REGISTER WITH MEMORY		8	32	22.4
	1	LMR	LOAD MEMORY WITH REGISTER		7	28	19.6
	2	LMI	LOAD MEMORY IMMEDIATE		9	36	25.2
ALU	1	ALR	ARITHMETIC OR LOGICAL REGISTER TO REGISTER A		5	20	14.0
	1	ALM	ARITHMETIC OF LOGICAL MEMORY TO REGISTER A		8	32	22.4
	2	ALI	ARITHMETIC TO LOGICAL SECOND WORD TO REGISTER A		8	32	22.4
	1	ROT	ROTATE REGISTER A		5	20	14.0
ADDRESS	3	JMP	JUMP CONDITIONAL	JUMP	11	44	30.8
				NO JUMP	9	36	25.2
	1	RET	CONDITIONAL RETURN FROM SUBROUTINE	RETURN	5	20	14.0
				NO RETURN	3	12	8.4
	1	RST	RESTART, SAVE ADDRESS		5	20	14.0
I/O	1	INP	INPUT FROM I/O		8	32	22.4
	1	OUT	OUTPUT TO I/O		6	24	16.8
	1	HLT	HALT		3	12	8.4

Table 1. Time State Comparison

4. Power Requirements

The power requirements of the MPS 803 are +5 volts at 2 Amps maximum and -10 volts at 750 milliamps maximum. This is but one input to the total power required, which determines the choice of power supplies. Other power requirements are given with their respective modules.

B. SIGNAL PROCESSING MODULE(SP) (SEE FIGURE II.-1 APPENDIX II.)

Knowing that the MPS 803 operates on 8 Bit digital inputs, the next consideration is the processing of multiple analog voltage signals to produce acceptable 8 bit digital signals.

1. Analog to Digital Converter (ADC)

The major component of the SP module is the ADC. Complete specifications for individual ADC's may vary; however, major inputs and outputs common to most ADC's and essential to system design are as follows:

a. Input Signal

Most ADC's require a relatively stable voltage input during the conversion time. This requirement can be met for rapidly changing signals through the use of a Sample and Hold component (SHA). Thus, the SHA becomes another design consideration.

b. Convert Signal

Most ADC's require an input pulse commanding the component to convert the given analog voltage to a parallel digital equivalent.

c. Busy Signal

Since conversion takes a finite period of time (20 micrcseconds for Midas FLD), an output signal indicating

that the ADC is in the process of conversion, but not complete, is available. It is fed to both the SHA and the MPS 803, and its functions will be described in the sections dealing with the SHA and the Midas FLD system program respectively.

d. Data Output

The data corresponding to the converted analog signal consist of a number of lines that indicate logical "1" or "0" and are the binary representation of the analog signal. For Midas FLD there are 8 such lines and they constitute the total input to a single port of the MPS 803, leaving 20 lines available for assignment to other input or output signals (such as convert, busy, etc.). Midas FLD utilizes one of the eight input lines for the "sign" and the remaining seven lines allow a resolution of two to the seventh power or 1/128 of full scale. (For Midas FLD this is .072 volts).

2. Sample and Hold (SHA)

The SHA component monitors a single incoming signal and, upon command, registers and outputs the value of the signal at that particular instant. The command for the SHA is the "Busy" signal of the ADC. When the ADC outputs a "busy" (logical "1" on the "Busy" line), the SHA holds the value of the input signal at that instant for the ADC to convert to its digital equivalent. When the ADC is not busy (logical "0" on the "Busy" line), the output voltage of the SHA is allowed to vary with the input signal.

Because the SHA only monitors one signal at a time, a multiplexer is required in the system to create the 8-channel capacity.

3. Multiplexer (MPX)

The multiplexer selects one of eight inputs and

places the input signal on the output line. The selection of input is controlled by a three-line signal to the MPX. Specific combinations of locical "ones" and "zeroes" on these lines select the input to be monitored. The lines correspond to binary numbers such that a combination of "000" selects input "0" and a combination of "111" selects input "7". These signals could be furnished directly from the MPS 803; however, in the interest of conserving the limited outputs, an integrated circuit "binary up-down counter" is utilized.

4. Binary Up-Down Counter

The binary up-down counter requires two input signals, "increment" and "reset", and has three outputs [Signetics, 1972]. Upon receiving a signal on the "reset" line, all output lines are set to logical "0" (output 000). Upon receiving an "increment" signal, one output line is set to logical "1" (output 001). Successive increment signals produce 010, 011, 100, 101, 110, and 111 as outputs. Thus, the "reset" and "increment" lines from the MPS 803 effectively select the analog signal that is the output of the MPX. A "Signetics 74193N" chip is used in Midas FLD for this purpose.

5. Components of the SP module require +15 volts at 54 milliamps, -15 volts at 54 milliamps and +5 volts at 200 milliamps, which is another input to the power module.

C. RECORDING MODULE

The Midas FLD recording module consists of the recorder and its associated accessories. The requirement that the recorder be as small as possible motivated an investigation of the Micro Communications "Microvox" recorder (Micro Communications Corp., 1975).

1. Microvox Recorder

The main design considerations of the recorder center around its input and output requirements. Most recorders require the following signals:

a. "On"

A logical "1" on the "on" line starts the motor.

b. "Clock"

Since the data written on the tape must be separated into distinguishable blocks, a high frequency, oscillating signal is input and written on the tape on a separate channel from the data. Any simple combination of data flow and corresponding clock oscillations can be incorporated. In the Microvox the clock oscillates between logical "1" and "0" at a rate of 1000 Hz. When the clock changes from "0" to "1", a bit of data is written on the tape. When the clock changes from "1" to "0" the next data bit is input by the MPS 803 and subsequently recorded on the next clock change from "0" to "1".

c. "Ready"

Since it takes the motor a finite amount of time to reach the proper drive speed, a "ready" signal is output which will not allow data to be written on the tape unless the recorder is "ready".

d. "Data"

The data line allows the input of data one bit at a time, which must correspond to the previously mentioned changes in the clock. Midas FLD controls this correspondence by monitoring the clock on one input line of the MPS 803 and changing the bit of data on the output line when the clock changes from "1" to "0" (see BIT$RECORD part

IV.).

With these signals in mind, Midas FLD is designed such that when the recorder is ready and the clock signal goes from "1" to "0", the data to the recorder are changed. To conserve input lines, the "ready" and "clock" signals are monitored through a logical "and" gate requiring only one MPS 803 input line.

e. Power

The microvox requires 100 milliamps at 12 volts and 60 milliamps at 5 volts which is another input to the power module design.

A photograph of the microrecorder appears in Figure II-3 of Appendix II.

D. PERIPHERAL ACCESSORIES MODULE

At this point practical considerations dictate the addition of a module that will allow separate identification of particular Naval aircraft to be printed on the wafer. This is accomplished through the implementation of Amp Industries Thumbwheel Switches.

1. Thumbwheel Switches

Thumbwheel switches chosen for Midas FLD are simple, reliable devices requiring one input and producing four outputs.

a. Input

The input to the thumbwheel switch is a power line which activates the outputs and provides the power to drive them.

b. Outputs

The outputs from the thumbwheel switches consist of four lines per switch and vary according to the choice of switch position. Those chosen for Midas FLD have "complemented" BCD output. That is, the output on the four lines consists of logical "1's" and "0's" arranged so that "1111" corresponds to "0" and "1110" to "1", "1101" to "2", and so on up to "0110" corresponding to "9". The fact that the outputs are complemented adds to system reliability and is another consideration for the system computer program. The outputs from the switches constitute 4 input lines to the MPS 803.

2. Switch Organization

Midas FLD incorporates six thumbwheel switches corresponding to the six digits in an aircraft bureau number. The individual activation of thumbwheel switches is accomplished through the use of a "Signetics 7442N BCD to Decimal Decoder."

a. BCD to Decimal Decoder Requirements

The BCD to decimal decoder requires four inputs consisting of lines carrying logical "1" or "0" levels. Their arrangement constitutes a binary coded digit such that "0000" corresponds to "0" and "1001" corresponds to "9" . A given arrangement of input signals activates one of ten output lines. Each of the first six output lines is connected to a thumbwheel switch and the inputs are four lines from one output port of the MPS 803. Thus, with output signals from the MPS 803 one can select the thumbwheel switch to be read.

3. External Switches

Further practical considerations dictate addition of two mechanical switches. One indicates when header

information is to be written on the tape; i.e., after the changing of tapes. The other signals the recording of information prior to turning off aircraft power. It is envisioned that this second switch be the "weight on wheels" switch already existing on aircraft. The operation of these switches is discussed further with the Midas FLD system computer program.

E. SYSTEM BLOCK DIAGRAM

Figure 1. shows the signal requirements for the various components of Midas FLD. This figure is helpful in writing the system program. It provides one of the major considerations for hardware adaptation, namely the MPS 803 input-output requirements. It is evident that there are 16 input signals and 9 output signals. Thus ports "0" and "1" are designated input ports and ports "2" and "3" are designated output ports with the corresponding simple hardware modifications being made. A notable consequent restriction is that two 8-line ports are fully occupied with inputs, while the remaining 8-line port and the 4-line port dedicated to output have only 9 output signals. Thus Midas FLD can accomodate 3 more outputs for additional information, but no more inputs can be accomodated.

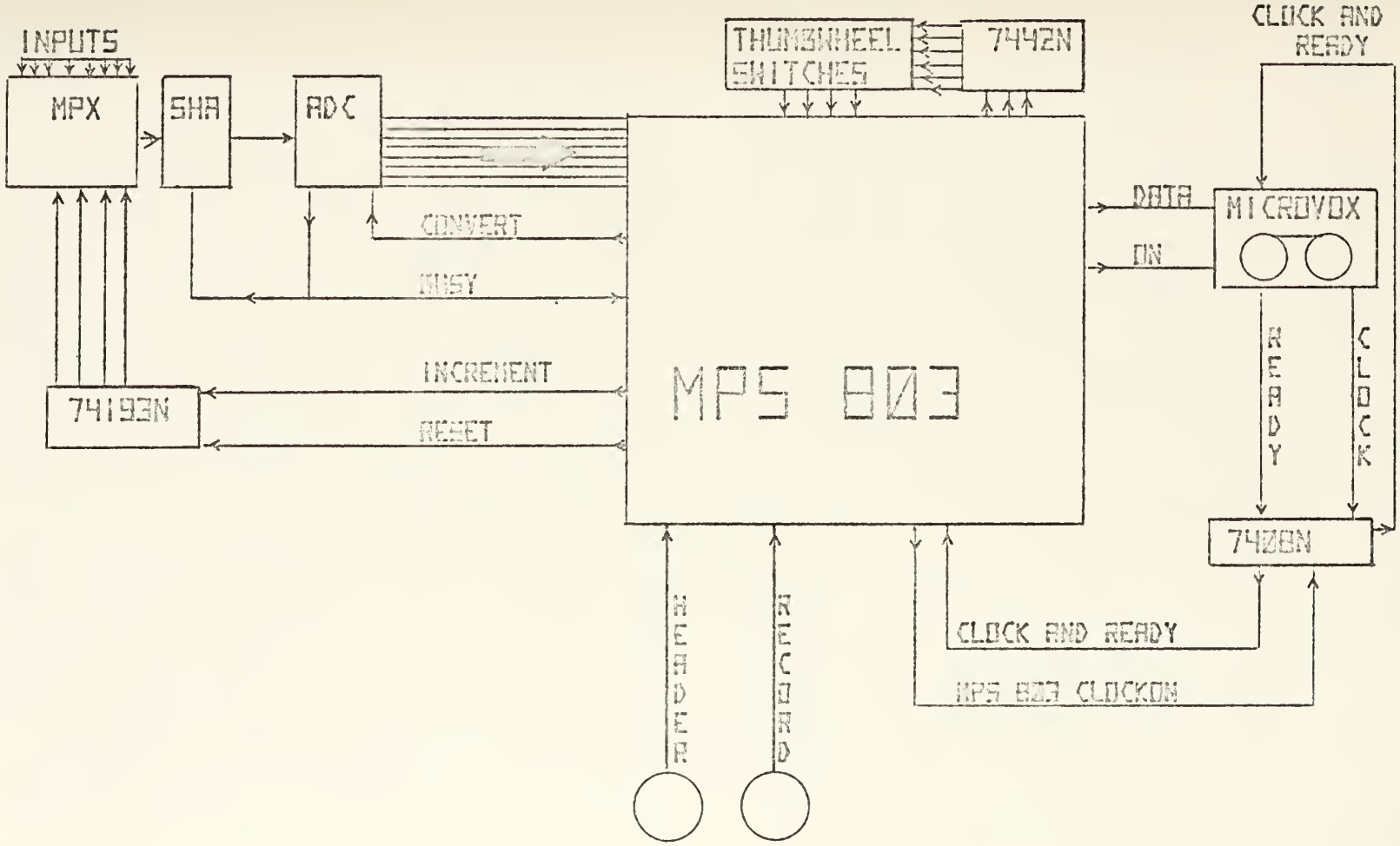

FIGURE 1. MIDAS FLD SYSTEM BLOCK DIAGRAM

III. INPUT-OUTPUT REFERENCING

To assist in understanding the Midas FLD computer program, a brief description of input-output line referencing is offered.

The 28 input-output lines of the MPS 803 are arranged in three 8-line ports and one 4-line port. These ports are numbered "0" through "3". Midas FLD ports "0" and "1", containing eight lines each, are dedicated input ports and ports "2" and "3", containing 8 and 4 lines respectively, are dedicated output ports. In the high level PLM language, a port is either input or output with the command "=INPUT(0)" for input port "0" or "OUTPUT(2)=" for output port "2". For input commands the signals on all eight lines of the port, consisting of logical "1's" and "0's", are read simultaneously. For output commands the desired combination of signals is placed on all eight lines according to the value of the right hand side of the equation.

Individual lines of input or output ports are referenced according to their position in the port by their positional binary value. A diagram of one port and its corresponding binary line values appears in Figure 2. Thus the command "OUTPUT(2)=1" puts a logical "1" on line "1" and "0's" on all other lines of output port 2. "OUTPUT(2)=64" puts logical "1" on line "7" and "0's" on all others. To output signals on more than one line at a time, add the binary values of those lines and command the output to be that total value; i.e., to output signals on lines 7,5, and 3, the number is 64+16+4=84, and the command is "OUTPUT(2)=84".

Input ports have the value of the signals on their input lines. Thus if lines 7, 5, and 3 of input port "0" had logical "1" levels and all other lines logical "0", then the command "A=INPUT(0)" would assign the value 84 to the

variable A.

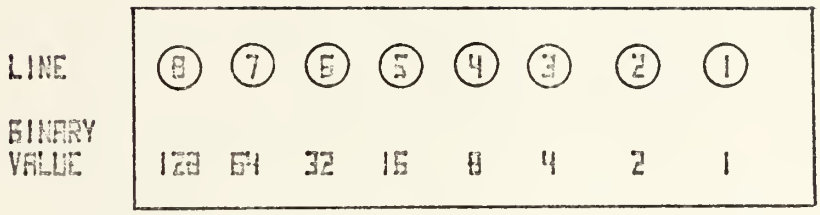

Figure 2. Input-Output Port

IV. SYSTEM COMPUTER PROGRAM

Knowing the signals required for the various components, attention is turned to the order and generation of these signals which will accomplish the proper data processing. It is here that Midas FLD becomes dedicated to the fatigue life data problem.

The Midas FLD system computer program generates the required signals in the proper sequence for effectively sampling the 8-channel multiplexed inputs. In addition it compares sequential information for each channel, and if any comparison meets the filter condition, all eight channels of information are recorded. This assumes that the signals being monitored are in phase with each other. Should subsequent research discover that there exists a time difference between the separate input channels, the program will have to be modified.

The development process for implementing this follows a logical sequence: first the generation of the input routine; followed by the filter routine; then the storage routine; and finally the recording routine. Once this main program is working, peripheral routines for unique signals may be added. (Thumbwheel switch information recording is an additional routine for Midas FLD).

A. DATA MONITORING SIGNAL SEQUENCE

The data monitoring signal sequence generates the following signals which store the eight values of the input channels in a vector, X(8):

1. Reset Multiplexer

To reset the multiplexer to channel"0" a pulse is applied to the 74193 chip. Since line 7 (64) of output port

2 is dedicated to "reset" of the 74193 chip, the program statements supplying the pulse are "OUTPUT(2)=64" followed by "OUTPUT(2)=0". This puts logical "1" on line 7 and logical "0" on all other lines. "Output(2)=0" returns line 7 to logical "0" effectively supplying a pulse on the 7 line.

Resetting the multiplexer places the analog signal from channel 1 on the output line of the multiplexer and concurrently on the lines of the Sample and Hold component.

2. ADC Conversion

The MPS 803 next signals the ADC to convert the analog signal to its digital equivalent. Line 1 of output port 2 is dedicated to the "convert" signal; thus the corresponding commands are "OUTPUT(2)=1" and "OUTPUT(2)=0". This puts a pulse on line 1 of output port 2 causing the ADC to make the conversion.

3. Wait

The MPS 803 then waits until an "End of Convert" or "not busy" signal is received from the ADC. Line 8 (128) of input port 1 is dedicated to "not busy" from the ADC; thus Midas FLD waits until INPUT(1)=128. The PLM command that more efficiently accomplishes this and thus appears in the input routine, is "(ROL(INPUT(1),1))".

4. Read

The MPS 803 reads this value of the first channel and stores it in X(1). The first channel's digital value is input on the eight lines of input port "0", and the command is "X(1)=INPUT(0)".

5. Increment Multiplexer

"Increment the multiplexer", to place the next channel's signal on the input lines, is the next command

from the MPS 803. Line 8 (128) of output "2" is dedicated to "increment", and the command sequence is "OUTPUT(2)=128" followed by "OUTPUT(2)=0". This pulses the 74193 chip causing the multiplexer to cycle to the next channel.

At this point control is passed to step 2, and the read process is repeated, incrementing the I variable to store the subsequent channel information in X(I+1). This loop is repeated eight times storing the eight channels of information. This procedure is labeled "MUX" for multiplexer and is accessed by the command "CALL MUX".

B. DATA FILTERING

Filtering of a vector starts with the reading of the vector and ends with the storing of the vector, if it is strain significant, in this manner:

1. DX Computation

The MPS 803 subtracts the vector from the last vector and stores the results in a change vector, DX(I), if this is not the first vector read:

```
DX(J)=XJ-XLSTJ;
```

where the J's are used to facilitate looping. Because the MPS 803 has no capability for storing negative numbers, the sign associated with DX(I) is stored in a separate vector labeled "SIG(I)". (The term "SIGN" cannot be used as it is a reserved word in PLM):

```
IF XJ>XLSTJ THEN DO;
    SIG(J)=1;
      END;
    ELSE DO;
  DX(J)=XLSTJ-XJ;
    SIG(J)=0;
      END;
```

2. Filter Condition

If the value of the last vector is outside the threshhold limits and the sign of the last change, SIGN1(K), is opposite the sign of this change, SIG(K), then store all XLST(K) as strain significant points. This is the most complicated logical statement of the entire program, and it reads:

```
IF(((XLSTJ>THRSHLD) OR (XLSTJ<MTHRSHLD)) AND ((SIG(K) XOR
                SIGN1(K))>0)) THEN GOTO STORE;
```

It successfully filters out all high frequency vibration points within the threshhold limits which are +10%, -5%; however, this is a variable that can be set at any desired level through the program.

3. MINDX

If the change DX(I) is more than 5% of full scale, then values are shuffled as in step 4 (5% change is signaled by the value of MINDX being met):

```
IF MINDX THEN GOTO SHUFFLE;
```

4. SHUFFLE

Shuffling of data places the current eight elements of input, X(8), into the comparison vector, XLST(8), and the current sign, SIG(8), into a comparison sign vector, SIGN1(8), as follows:

```
SHUFFLE:DO J=0 TO 7;
    XLST(J)=X(J);
    SIGN1(J)=SIG(J);
    END;
```

A practical consideration of note is that only the vector subtraction X(I)-XLST(I) need be bypassed for the first vector input (at this point there is no XLST(I)) since

the threshhold criteria will cause the shuffling of previous data and generate future comparison values of SIGN1(I). The sequence of executing the filter condition and then applying the MINDX criteria is essential in order to filter before shuffling.

5. Data Storage

Storage of data vectors is performed in the loop labeled "STORE:" as referred to in step 2 of this section. "STORE" transfers the "strain significant vector" from the XLST(I) vector to the temporary memory buffer. The temporary memory buffer is given the name VECTORS and is capable of storing 224 strain significant vectors. The loop that stores XLST(I) in VECTORS is:

```
STORE: DO I=0 TO 7;
VECTORS=XLST(I)+SIGN1(I);
UNIT=UNIT+1;
```

It is noted that the "+ SIGN1(I)" places the sign of the slope of XLST(I) in the right most binary digit. As each element of a vector is stored, the element count is incremented:

```
ELEMENT=ELEMENT+1;
```

When the temporary memory storage of vectors is full; i.e., when it has 224 vectors or 1792 elements, all elements are recorded:

```
IF ELEMENT=1792 THEN GOTO RCD;
RCD:CALL RCDR(ELEMENT);
```

C. DATA RECORDING

Recording of filtered vectors stored in temporary memory is accomplished in a procedure labeled "RCDR".

1. "RCDR"

"RCDR" first turns the recorder and its clock on. Since lines 16 and 32 of output port 2 are dedicated to the recorder "ON" and "CLOCK", the command that accomplishes this is:

```
OUTPUT(2)=48;
```

After initializing the index, "unit", to the first element of the memory storage, "vectors", RCDR enters a loop that records each element through the use of a procedure labeled "BIT$RECORD":

```
LOOP:DO N=0 TO 7;
CALL BIT$RECORD(VECTORS);
```

As each element is recorded, the element index is incremented:

```
UNIT=UNIT+1;
```

so that the memory is recorded sequentially, preserving the sequence of the original data.

If the index "unit" is less than the number of elements stored, then eight more elements are recorded:

```
IF (UNIT-0900H)<ELEMENT THEN GOTO LOOP;
```

The "GAP" procedure is included to facilitate data retrieval. The retrieval, or read, system will necessarily read a block of data, 1792 elements, stop the recorder and transfer this data to a larger capacity computer. Subsequently, the read system will start and stop the recorder to retrieve sequential blocks of data. This starting and stopping of the recorder motor will create gaps of unknowr length in the reader. To assure that gaps written on the tape by the write system are longer than these reader gaps (since no two motors are identical in speed there will be some difference, and if the gaps written on the tape were not sufficient to compensate for this difference, data would be lost) an additional gap is written on the tape through the use of the procedure "GAP".

2. "GAP"

The "GAP" procedure interrupts the "clock" signal to the recorder; thus writing the unique "bias" signal onto the tape. From the signal description in part 1 of this section, OUTPUT(2)=16 accomplishes this. The variable length time delay feature of the PLM compiler is then utilized to acccunt for the length of the gap, "CALL TIME(I)". After this time delay the clock signal is restored, "OUTPUT(2)=48".

3. "BIT$RECORD"

The "BIT$RECORD" procedure takes the eight binary digits of one vector element and records them, one at a time, onto the tape. This is accomplished with eight passes through a loop:

```
DO I=1 TO 8;
```

Each pass first places the right most binary digit (logical "1" or "0") on the recorder data line:

```
OUTPUT(3)=BIT AND 1;
```

"BIT$RECORD" then delays until the "clock" signal transitions from a logical "0" to logical "1" indicating that the digit has been read by the recorder:

```
DO WHILE NOT(ROL(INPUT(1),2));
END;
```

A second delay waits until the "clock" transitions from logical "1" to "0":

```
DO WHILE ROL(INPUT(1),2);
END;
```

At this point the next binary digit is rotated into the rightmost position, this is the "ROR" portion of the data output instruction:

```
BIT=ROR(BIT,1);
```

It is noted that "BIT$RECORD" is a unique procedure designed for use with the Microvox recorder (arrangement of clock pulses, number of data lines, etc.). Use of other recorders would require modification of this procedure.

D. PERIPHERAL ROUTINES

1. "Read"

One of the peripheral routines presently incorporated in the Midas FLD system computer program is the procedure for reading the thumbwheel switches, "READ".

"Read" effectively activates the proper thumbwheel switch by placing the value of the variable "C" on "OUTPUT(2)". Since lines 2 (2), 3 (4), and 4 (8) are dedicated to selection of thumbwheel switches through the 7442 chip, whenever OUTPUT(2) is increased by 2, the next thumbwheel switch will be activated. The command sequence:

```
OUTPUT(2)=C;
C=C+2;
RETURN (INPUT(1) AND 15) XOR 15;
```

steps through the thumbwheel switches.

Storage of thumbwheel switch information is performed in the loop:

```
DO I=1 TO 8;
IF I<6 THEN VECTORS=128;
ELSE VECTORS=SHL(READ,4)+READ;
UNIT=UNIT+1;
END;
```

It is noted that the first 5 elements of the thumbwheel vector are 128. This is done to distinguish the

thumbwheel switch information from data vectors. Thumbwheel switch information, being only 4 lines of data, can be arranged with two thumbwheel switches per element of the vector. Information from the six thumbwheel switches occupy the next three elements, two switches per element.

2. "DELAY"

Practical considerations dictate the addition of another peripheral routine, "DELAY". This routine, the logic of which is too involved to explain here, effectively waits 20 seconds after the record button is depressed before recording the data vectors. Each second during the wait the record button is rechecked, and if it has returned to the undepressed position, data processing is resumed.

The record button is envisioned to be a "weight-on-wheels" or "landing" switch. The delay loop allows touch-and-go landings without loss of data monitoring with the 20 second delay being a nominal provision for landing roll out before recording data vectors.

The Midas FLD system computer program block diagram is shown in Figure 3, and the program itself is given in Appendix I.

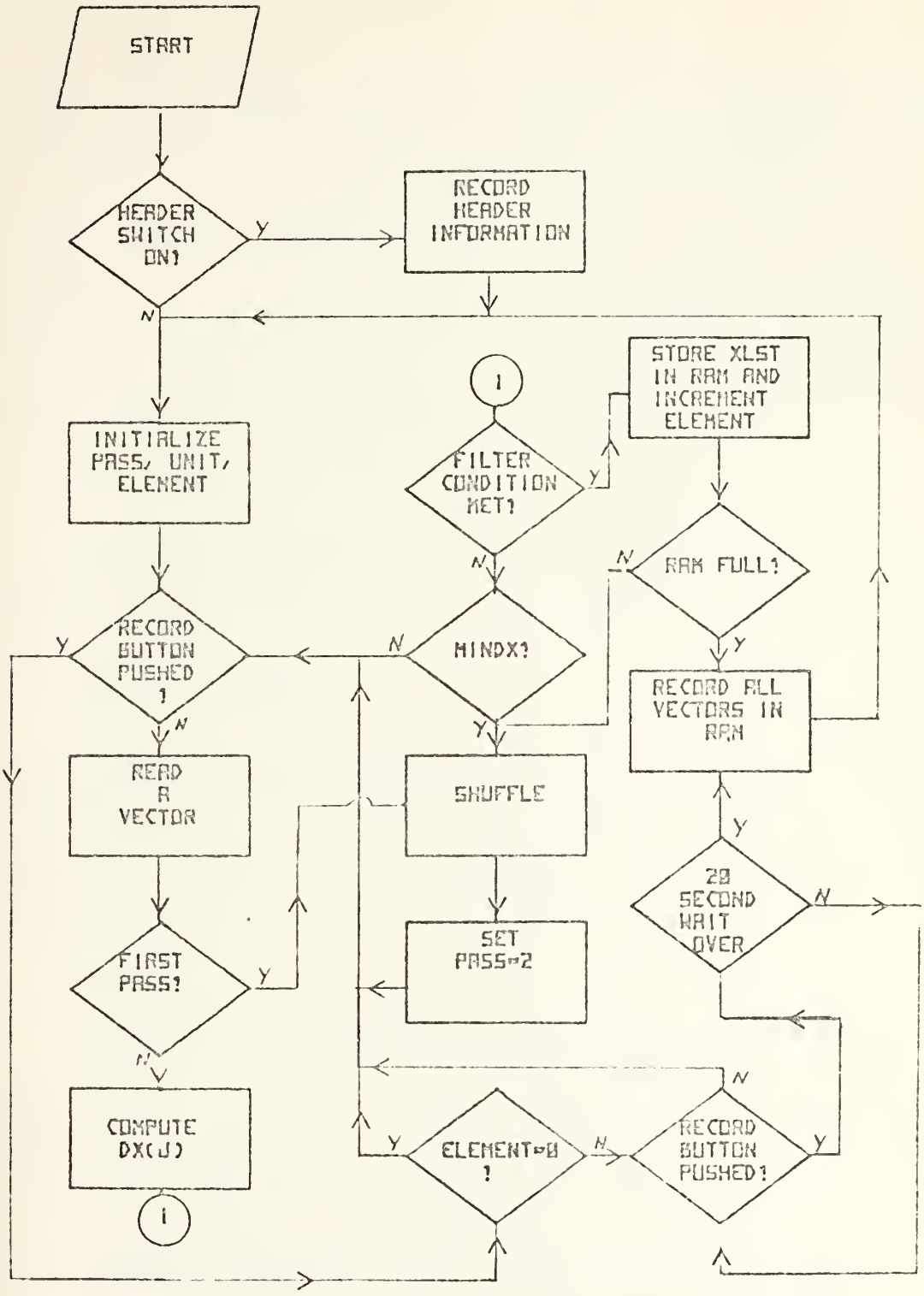

FIGURE 3.
MIDAS FLD PROGRAM BLOCK DIAGRAM

V. SYSTEM TESTING

Due to the modular design of Midas FLD, it is possible to test each module once it has been assembled. This facilitates the isolation and correction of errors.

A. SIGNAL PROCESSING TEST

Testing of the signal processing module involves connection of all voltage supplies and simulation of input and control signals. This is most readily accomplished through a temporary electrical circuit "breadboard".

1. Power Supplies

Appropriate power supplies are connected to the signal processing module. The voltage requirements of the Midas FLD signal processing Module are +5V, +15V, and -15V.

2. Input Signals

In order to ensure that the analog to digital conversion of signals is correct, known constant voltages are attached to the inputs of the module. The voltages for Midas FLD are .024V for an equivalent zero output and 4.996V for an equivalent full-scale positive output.

3. Control Signals

Most of the elements require 5 volt logic pulses for their control, and the delicacy of the electronic elements requires the use of a pulse generator to control the functions of "Channel Increment" and "Clear" of the 74193, and "Convert" commands to the digital converter.

4. Output Signals

Outputs of the signal processing module are monitored with lights attached to each of the eight output lines. Upon activating the pulse generator, the eight lines of digital output are observed as they represent the known

voltage inputs of the various channels. This completes the testing of the signal processing module.

B. PERIPHERAL ACCESSORIES MODULE TEST

Testing of the peripheral accessories module is accomplished in three phases: 1) thumbwheel switch selection, 2) thumbwheel switch output, and 3) recorder signal processing.

1. Thumbwheel Switch Selection

After proper voltage supplies are connected, as in the signal processing module test, distinct "binary coded digits" are supplied to the 7442 via the three binary input lines. The signals on these lines are controlled through the breadboard to select thumbwheel switches 1,2,3,4,5, and 6 respectively. The six output lines of the 7442 are observed to be activated according to the "binary coded digit" applied at the input.

2. Output Verification

After switch selection has been verified, each thumbwheel switch is individually selected and its outputs observed.

3. Recorder Observation

Recorder signal processing is more readily observed during total system test; thus its testing is deferred.

C. TOTAL SYSTEM TEST

Were the Midas FLD more complicated in design, a test of the program in the MPS 803 would be warranted including simulation of the signal processing and peripheral accessories modules. However, since Midas FLD is relatively simple, testing of this module is foregone, and the entire system is assembled utilizing the breadboard.

1. Inter-module Connections

Connections between the signal processing module, MPS 803, and the peripheral accessories module are made through the wire-wrapped pins on the back of the card cage housing these modules. Connections between the power supply and the recorder modules are made via the temporary breadboard.

2. Input Signal Simulation

To simulate the strain gage signal input, a sine wave generator is connected via the intermediate breadboard to the input of the signal processing module. The frequency of this signal is known; thus, the filtering portion of the MPS 803 program is tested by measuring the actual time required to filter the signal, activate the recorder, and record it. For a 4 cycle per second signal it should take Midas FLD approximately 28 seconds to activate the recorder. It should take Midas FLD approximately 16 seconds to record the filtered signal.

3. Program Observation

To observe the program functioning necessitates the use of a Pro-Log M-821 Tester [Pro-log Corporation, 1974]. This attaches to the central processing unit of the MPS 803 and is capable of displaying the machine code instruction of the system program that is being executed along with any input or output data on the input-output ports.

Utilizing the "run" and "cycle" modes of the M-821, it can be determined if the logic of the Midas FLD system program is functioning properly. The program can be stopped at every output step, and actual output and input signals can be traced and verified. It is at this point that the deferred testing of the recorder module is accomplished.

As the program reaches the record procedure, the cycle mode on the M-821 tester is entered. The program execution is cycled through steps which activate certain portions of the recorder. The output signals are verified at the output port with a digital voltmeter to insure proper functioning of the MPS 803. They are then monitored with the digital voltmeter to insure proper functioning of the microrecorder.

Once it is determined that the system is performing within tolerance of the time limits, the temporary breadboard connections can be replaced by permanently soldered connections.

Upon completion of this permanent wiring, Midas FLD is ready to produce the tape of data vectors.

VI. OBSERVATIONS

Midas FLD represented the state-of-the-art in microprocessors at the outset of its development. It is noted that this field is rapidly advancing, and during development the 8008 CPU has been twice displaced by newer , higher level and more efficient CPU's. Its first successor, the 8080, is currently a proven workhorse in many development systems. The next model, just now reaching the market, will no doubt exhibit similar improvements over the 8080.

These advances will allow more flexibility in reprogramming Midas FLD. In particular, it is expected that all analog signals might not be in phase (an assumption on which Midas FLD is based), necessitating a major reprogramming. At the present time Midas FLD does not have the PROM capacity to handle this; however, an 8080 CPU takes only 80% of the instructions to accomplish what Midas FLD's 8008 does. The additional 20% of instruction space could be utilized in expanding the system to accomodate individual channel monitoring.

Also, the time state of an 8080 is .45 microseconds compared to 2.8 microseconds for Midas FLD's 8008. Preliminary observations indicate that the frequency limit for Midas FLD's monitoring is 40 hertz. With an 8080 this would be increased, due to the improved time state, to approximately 250 hertz.

Midas FLD's Microvox recorder is somewhat more advanced in relation to the state-of-the-art than the 8008. Close consultation during development with Mr. Joe Mozer of Micro Communications Corp. was maintained because the Microvox was not a proven device at the outset of Midas FLD's development. Subsequent recorder development, concurrent

with Midas FLD's development was experienced and the Microvox is now an acceptable component. It is noted, however, that this field is also advancing, and the successor to the Microvox is expected to be marketed in the near future. This successor will be of greater capacity and take less time to record the temporary memory.

The areas of the ADC, MPX, SHA, thumbwheel switches and remaining electronic components have not experienced such technological advances, and it is felt they are state-of-the-art components.

Reliability of most components is good with two exceptions; first the card upon which the 8008 is mounted and second the power supply. Normal laboratory handling caused the failure of the CPU card and the +5 volt power supply. It is felt that the CPU card failure was an isolated occurrence not likely to occur again; however, less is known about the power supply failure, and a continuing investigation of power supplies is recommended. Preliminary investigation of power supplies indicates that solid-state modules lack the amperage capacity required by Midas FLD. State-of-the-art encapsulated supplies currently can supply a maximum of one amp at 5 volts, and Midas FLD requires three amps from the 5 volt supply. For this reason Midas FLD currently runs on temporary laboratory power supplies.

Midas FLD focuses on systems based around Intel Corporation products. Other leaders in this field include Fairchild Electronics, Texas Instruments and Motorola. It is expected that any one of these companies would be capable of developing, producing and hardening a system for use in Naval aircraft.

```
DECLARE DCL LITERALLY 'DECLARE';
DCL LIT LITERALLY "LITERALLY";
DCL BT LITERALLY 'BYTE';
DCL (I,K,J,N,S,P,T) BT;
DCL L ADDRESS;
DCL BIT BT;
DCL MINDX BT;
DCL X(8) BT;
DCL DX(8) BT;
DCL XLST(8) BT;
DCL SIG(8) BT;
DCL C BT;
DCL UNIT ADDRESS;
DCL EXCEEDED LIT '255';
DCL VECTORS BASED UNIT BT;
DCL SIGN1(8) BT;
DCL (XJ,XLSTJ) BT;
DCL THRSHLD LIT '140';
DCL MTHRSHLD LIT '120';
DCL ELEMENT ADDRESS;
BIT$RECORD:PROCEDURE(BIT);
DCL BIT BT;
DO I=1 TO 8;
OUTPUT(3)=BIT AND 1;
BIT=ROR(BIT,1);
DO WHILE NOT(ROL(INPUT(1),2));
END;
DO WHILE ROL(INPUT(1),2);
END;
END;
END BIT$RECORD;
GAP:PROCEDURE(I);
DCL I BT;
OUTPUT(2)=16;
```

```
CALL TIME(1);
OUTPUT(2)=48;
END;
RCDR:PROCEDURE(ELEMENT);
DCL (ELEMENT) ADDRESS;
DCL N BYTE;
UNIT=0900H;
OUTPUT(2)=48;
LOOP:DO N=0 TO 7;
CALL BIT$RECORD(VECTORS);
UNIT=UNIT+1;
END;
IF (UNIT-0900H)>ELEMENT THEN GOTO LOOP;
CALL GAP(7);
OUTPUT(2)=0;
END;
READ:PROCEDURE BYTE;
OUTPUT(2)=C;
C=C+2;
RETURN (INPUT(1) AND 15) XOR 15;
END READ;
MUX:PROCEDURE;
OUTPUT(2)=64;
OUTPUT(2)=0;
DO I=0 TO 7;
OUTPUT(2)=1;
OUTPUT(2)=0;
DO WHILE NOT(ROL(INPUT(1),1));
END;
X(I)=INPUT(0) AND 254;
OUTPUT(2)=128;
OUTPUT(2)=0;
END;
END MUX;
UNIT=0900H;
IF ROL(INPUT(1),3) THEN DO;
```

```
C=0;
DO I=1 TO 8;
IF I<6 THEN VECTORS=128;
ELSE VECTORS=SHL(READ,4)+READ;
UNIT=UNIT+1;
END;
CALL RCDR(8);
END;
DCL PASS BT;
PASS=1;
RUN:ELEMENT=0;
   UNIT=2304;
CHECK:IF(ROL(INPUT(1),4)) THEN GOTO RECORD;
CALL MUX;
IF PASS=1 THEN GOTO SHUFFLE;
MINDX=0;
DO J=0 TO 7;
XJ=X(J);
XLSTJ=XLST(J);
IF XJ>XLSTJ THEN DO;
DX(J)=XJ-XLSTJ;
SIG(J)=1;
END;
ELSE DO;
DX(J)=XLSTJ-XJ;
SIG(J)=0;
END;
IF DX(J)>6 THEN MINDX=EXCEEDED;
END;
DO K=0 TO 7;
XLSTJ=XLST(K);
IF(((XLSTJ>THRSHLD) OR (XLSTJ<MTHRSHLD)) AND ((SIG(K) XOR
SIGN1(K))>0)) THEN GOTO STORE;
END;
IF MINDX THEN GOTO SHUFFLE;
GO TO CHECK;
```

```
STORE: DO I=0 TO 7;
VECTORS=XLST(I) +SIGN1(I);
UNIT=UNIT+1;
ELEMENT=ELEMENT+1;
END;
IF ELEMENT=1792 THEN GOTO RCD;
SHUFFLE:DO J=0 TO 7;
XLST(J)=X(J);
SIGN1(J)=SIG(J);
END;
PASS=2;
GO TO CHECK;
RECORD:IF ELEMENT=0 THEN GO TO CHECK;
DELAY:DO S=1 TO 20;
IF(NOT(ROL(INPUT(1),4))) THEN GO TO CHECK;
DO T=1 TO 35;
CALL TIME(200);
END;
END;
RCD:CALL RCDR(ELEMENT);
GO TO RUN;
EOF
```

APPENDIX II MIDAS FLD MODULE WIRING LISTS

The following are detailed wiring lists of laboratory constructed modules and descriptions necessary for reproducing them. For purposes of identification the following conventions apply:

SP-XX	Signal Processing module pin XX
SHA-XX	Sample and Hold component pin XX
ADC-XX	Analog to Digital Converter component pin XX
MPX-XX	Multiplexer component pin XX
TW-X	Thumbwheel Switch number X
4050-XX	CMOS buffer chips catalog number 4050, pin XX
7408-XX	Signetics 7408N "and" gate, pin XX
74193-XX	Signetics 74193 "Binary Counter", pin XX
7404-XX	Signetics 7404 Inverter chip, pin XX
IO-XX	Input-Output card, pin number XX
7442-XX	Signetics 7442 BCD to Decimal Decoder, pin XX
PA-XX	Peripheral Accessories module, pin XX

The following connections are made on the pin connectors of the Pro-Log card rack to interface the SP module to the remainder of the system:

SP-01,SP-02_____5 volt power supply
SP-03,SP-04_____ Ground
SP-07_____-15volt power supply
SP-08_____+15volt power supply
SP-10, SP-12, SP-14, SP-16, SP-18, SP-20, SP-22,
SP-24_____ Input Channels 7 thru 0 respectively
SP-19_____IO-41 Busy signal from ADC
SP-21_____IO-56 ADC Least Significant Bit
SP-23_____IO-54 " Bit 2
SP-25_____IO-52 " Bit 3
SP-27_____IO-50 " Bit 4
SP-29_____IO-48 " " 5
SP-31_____IO-46 " " 6
SP-33_____IO-44 " " 7
SP-35_____IO-42 ADC Most Significant Bit
SP-28_____IO-21 Convert line to ADC
SP-36_____IO-41 End of Convert Signal from ADC
SP-39_____PA-39 Thumbwheel no. 1 Line
SP-41_____PA-41
SP-43_____PA-43
SP-45_____PA-45
SP-47_____PA-47
SP-49_____PA-48 Thumbwheel no. 6 Line
SP-42_____IO-07 Channel Increment of 74193
SP-44_____IO-09 Channel clear of 74193
SP-46_____IO-19 Thumbwheel Select no. 1 (7442)
SP-48_____IO-17
SP-50_____IO-15 Thumbwheel Select no. 3

Inter-component connections of the SP module are as follows:

MPX-01_____SP-07
MPX-02_____SP-08
MPX-03_____SP-01
MPX-04_____SP-04
MPX-05_____SP-10
MPX-06_____SP-12
MPX-07_____SP-14
MPX-08_____SP-16
MPX-09_____SHA-06
MPX-10_____SHA-06
MPX-11_____SP-18
MPX-12_____SP-20
MPX-13_____SP-22
MPX-14_____SP-24
MPX-25_____MPX-26
MPX-27_____74193-06
MPX-28_____74193-03
MPX-29_____74193-02

SHA Connections

SHA-01_____SP-04
SHA-02_____SP-07
SHA-03_____SP-08
SHA-06_____MPX-09 and MPX-10
SHA-07_____ADC-37 and ADC-43
SHA-08_____SP-04
SHA-12_____ADC-02

ADC Connections

ADC-02_____SHA-12
ADC-03_____SP-04
ADC-04_____ Wiper of 200 Ohm adjusting potentiometer
ADC-06_____ End of 200 Ohm adjusting potentiometer
ADC-20_____ Wiper of 20 K-ohm adjusting resistor
ADC-21_____ADC-22

ADC-25_____ End of 20 K-ohm adjusting resistor and SP-07

ADC-27_____ Other end of 20 K-ohm adjusting resistor and SP-08

ADC-29_____SP-01

ADC-33_____SP-19

ADC-34_____SP-28

ADC-35_____ADC-36

ADC-37_____SP-36 and SHA-7

ADC-43_____SP-36 and SHA-7

ADC-56_____SP-21

ADC-58_____SP-23

ADC-61_____SP-25

ADC-63_____SP-27

ADC-65_____SP-29

ADC-67_____SP-31

ADC-71_____SP-33

ADC-72_____SP-35

74193 Connections

74193-02_____MPX-29

74193-03_____MPX-28

74193-04_____SP-01

74193-05_____7404-02

74193-06_____MPX-27

74193-08_____SP-04

74193-11_____SP-01

74193-14_____SP-44

74193-16_____SP-01

7442 Connections

7442-01_____7404-01

7442-02_____7404-03

7442-03_____7404-05

7442-04_____7404-13

7442-05_____7404-11

7442-06_____7404-09

7442-08_____SP-04
7442-12_____SP-04
7442-13_____SP-50
7442-14_____SP-48
7442-15_____SP-46
7442-16_____SP-01

7404 Pin Connections

The SP module incorporates two Signetics 7404n inverters whose purpose is to maintain the positive logic of the Midas FLD system. One 7404n is used to invert outputs of the 7442, and its connections are as follows:

7404-01_____7442-01
7404-02_____SP-39
7404-03_____7442-02
7404-04_____SP-41
7404-05_____7442-03
7404-06_____SP-43
7404-07_____SP-04
7404-08_____SP-49
7404-09_____7442-06
7404-10_____SP-47
7404-11_____7442-05
7404-12_____SP-45
7404-13_____7442-04
7404-14_____SP-01

The remaining 7404 is used to invert the increment pulse to the 74193, thus maintaining its positive logic, and the connections are as follows:

7404-01_____SP-42
7404-02_____74193-05
7404-07_____SP-04
7404-14_____SP-01

The 200 ohm adjusting potentiometer is the gain adjustment, and the 20 K-ohm adjusting potentiometer is the zero adjustment for the ADC. For zero adjustment, supply .024 volts to the input and adjust the potentiometer until the ADC output is "10000001" for bipolar operation. For gain adjustment, after completing zero adjustment, supply 4.996 volts to the input and adjust the potentiometer until the output of the ADC is "11111110".

The SP module appears in Figure II-1.

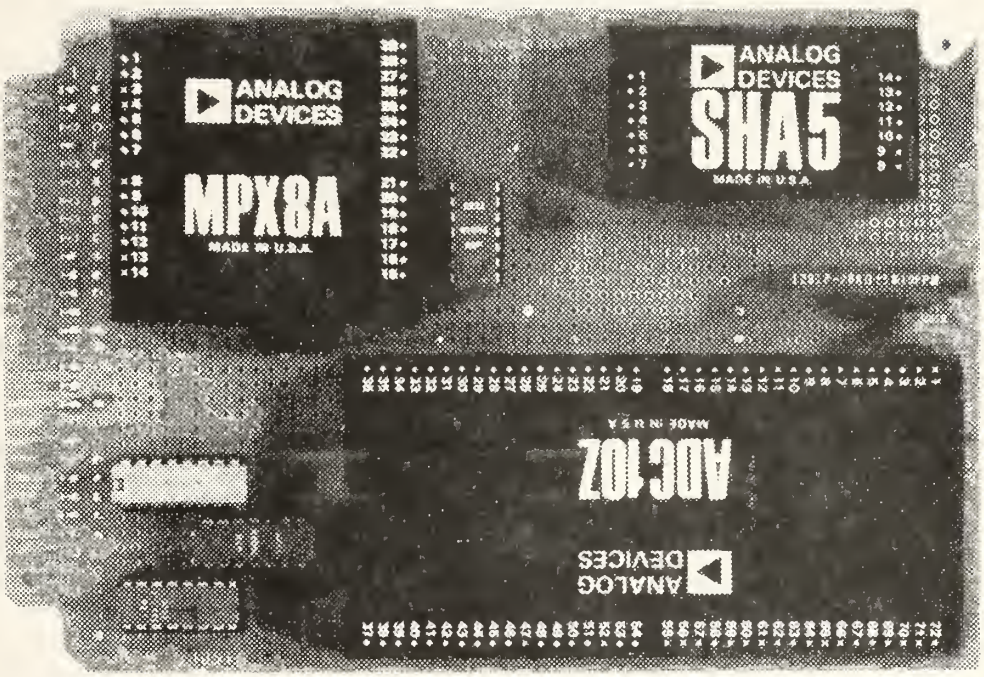

Figure II-1. Signal Processing Module

Input-Output Connections

The pin connectors for the Input-Output ports are located on the back of the Pro-Log card rack. Interface connections to other modules are as follows:

IO-07_____SP-42
IO-09_____SP-44 Channel Clear
IO-11_____PA-16 MPS 803 Clockon
IO-13_____ Pin Connector "A", Pin 5, Microvox Recorder
IO-15_____SP-46 Thumbwheel BCD no. 1
IO-17_____SP-48
IO-19_____SP-50 Thumbwheel BCD no. 3
IO-21_____SP-28 ADC Convert Signal
IO-24_____N. C. no connection
IO-26_____N. C.
IO-28_____N. C.
IO-30_____Pin Connector "A", Pin 2, Microvox Recorder
IO-41_____SP-36 ADC End of Convert Signal
IO-43_____PA-14 Recorder Clock and Ready
IO-45_____Input from "Header" Switch
IO-47_____Input from "Record" Switch
IO-49_____PA-49 Thumbwheel BCD no. 4
IO-51_____PA-51
IO-53_____PA-53
IO-55_____PA-55 Thumbwheel BCD no. 1
IO-42_____SP-35 ADC Bit no. 8
IO-44_____SP-33
IO-46_____SP-31
IO-48_____SP-29
IO-50_____SP-27
IO-52_____SP-25
IO-54_____SP-23
IO-56_____SP-21 ADC Bit no. 1

Peripheral Accessories Pin Connections

Like the Input-Output pins, Peripheral Accessories module pins are on the back of the Pro-Log card rack. Interface connections are as follows:

PA-10_____Pin Connector "B", Pin 16, Microvox Recorder
PA-12_____Pin Connector "B", Pin 15, Microvox Recorder
PA-14_____IO-43 Clock and Ready
PA-16_____IO-11 MPS 803 Clockon
PA-18_____Pin Connector "B", Pin 1, Microvox Recorder
PA-39_____SP-39 Thumbwheel no. 1 Power Line
PA-41_____SP-41
PA-43_____SP-43
PA-45_____SP-45
PA-47_____SP-47
PA-48_____SP-49 Thumbwheel no. 6 Power Line
PA-49_____IO-49 Thumbwheel BCD no. 4
PA-51_____IO-51
PA-53_____IO-53
PA-55_____IO-55 Thumbwheel BCD no. 1

Inter-component connections of the PA module are as follows:

Thumbwheel Switches

Thumbwheel switches each have four outputs consisting of an 8 line, a 4 line, a 2 line and a 1 line. Each of these lines is connected, through an isolating diode, to the same PA pin as the corresponding line on the other switches. The input, or power line, of each switch comes from its corresponding select line from the SP module. The connections are as follows:

TW-1 8 line to diode to PA-49
TW-2 8 line to diode to PA-49
TW-3 8 line to diode to PA-49

TW-4 8 line to diode to PA-49
TW-5 8 line to diode to PA-49
TW-6 8 line to diode to PA-49
TW-1 4 line to diode to PA-51
TW-2 4 line to diode to PA-51
TW-3 4 line to diode to PA-51
TW-4 4 line to diode to PA-51
TW-5 4 line to diode to PA-51
TW-6 4 line to diode to PA-51
TW-1 2 line to diode to PA-53
TW-2 2 line to diode to PA-53
TW-3 2 line to diode to PA-53
TW-4 2 line to diode to PA-53
TW-5 2 line to diode to PA-53
TW-6 2 line to diode to PA-53
TW-1 1 line to diode to PA-55
TW-2 1 line to diode to PA-55
TW-3 1 line to diode to PA-55
TW-4 1 line to diode to PA-55
TW-5 1 line to diode to PA-55
TW-6 1 line to diode to PA-55
TW-1 input to PA-39
TW-2 input to PA-41
TW-3 input to PA-43
TW-4 input to PA-45
TW-5 input to PA-47
TW-6 input to PA-48

Microvox Signals

Because the Microvox signals are of CMOS levels, they must go through a National Semiconductor 4050 buffer before being applied to Midas FLD's TTL inputs. This 4050 buffer and a 7408 "and" gate constitute the Microvox interface provisions, and the connections are as follows:

4050 Connections

4050-01_____PA-01
4050-02_____7408-13
4050-03_____PA-10
4050-04_____7408-12
4050-05_____PA-12
4050-08_____PA-04
4050-09_____PA-20

7408 Connections

7408-01_____PA-16
7408-02_____4050-02 and 7408-13
7408-03_____PA-18
7408-07_____PA-04
7408-11_____PA-14
7408-12_____4050-04
7408-13_____4050-02 and 7408-02
7408-14_____PA-01

The assembled PA module appears in Figure II-2.

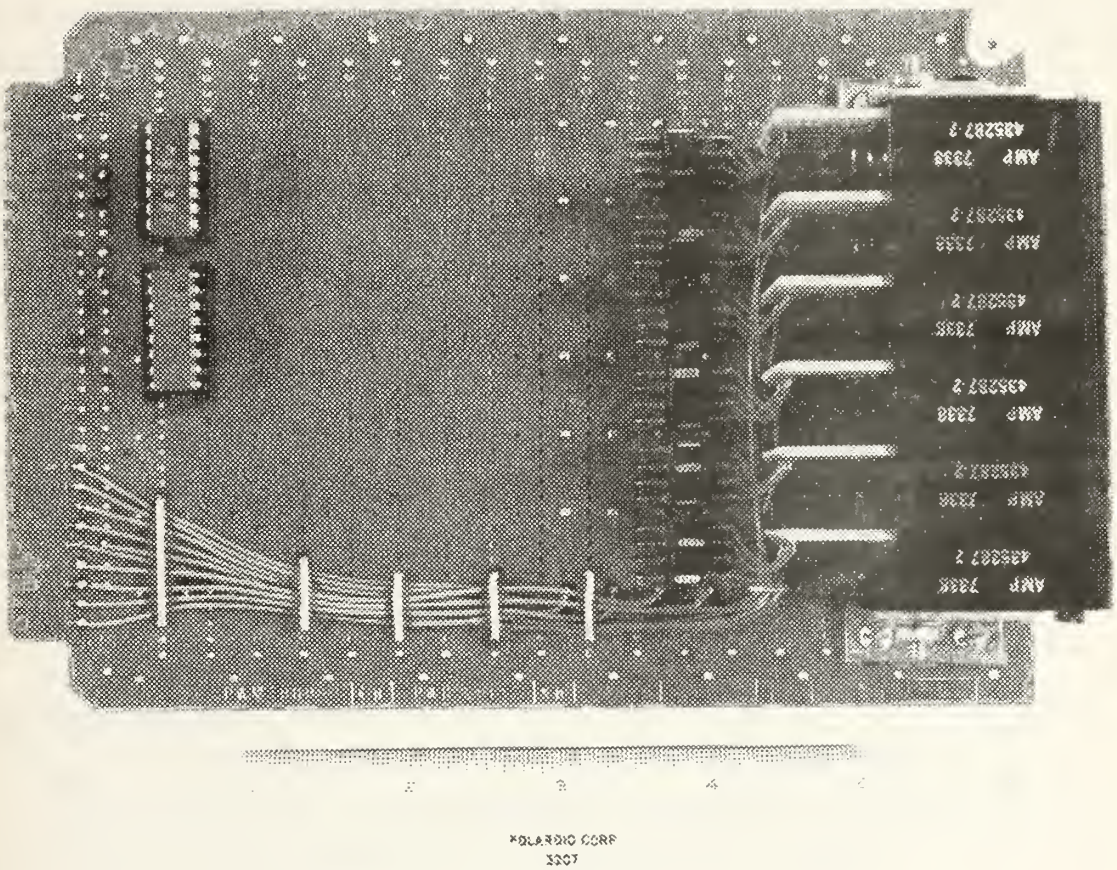

Figure II-2. Peripheral Accessories Module

Microvox Recorder Pin Connections

The recorder connections are made via two interconnecting cables of 16 lines each. They are labeled A1 through A16 for the first cable and B1 through B16 for the second cable. their connections are as follows:

A1,A2_____12 volt power supply
A5_____IO-13 On Signal
A7, A8_____Ground
A9, A10_____5 volt power supply
A11, A12, A13_____Ground
B1_____PA-18 Clock In
B2_____IO-30 Data
B14_____PA-20 End of Tape Signal
B15_____PA-12 Ready Signal
B16_____PA-10 Clock Out Signal

Internal modifications to the Microvox Recorder are: a 500 ohm resister between A4 and A7, and A16 shorted to A1.

The Microvox microrecorder appears in Figure II-3., a photograph of a wafer and a cassette in Figure II-4., and the assembled Midas FLD system in Figure II-5.

External Switches

The weight-on-wheels switch connects IO-47 to +5 volts when there is weight-on-wheels; otherwise it is connected to ground. The header switch is a single-pole-double-throw switch, and the pole is connected to IO-45. One side, the "write header" side,is connected to +5 volts, while the other side, "no header", is connected to ground.

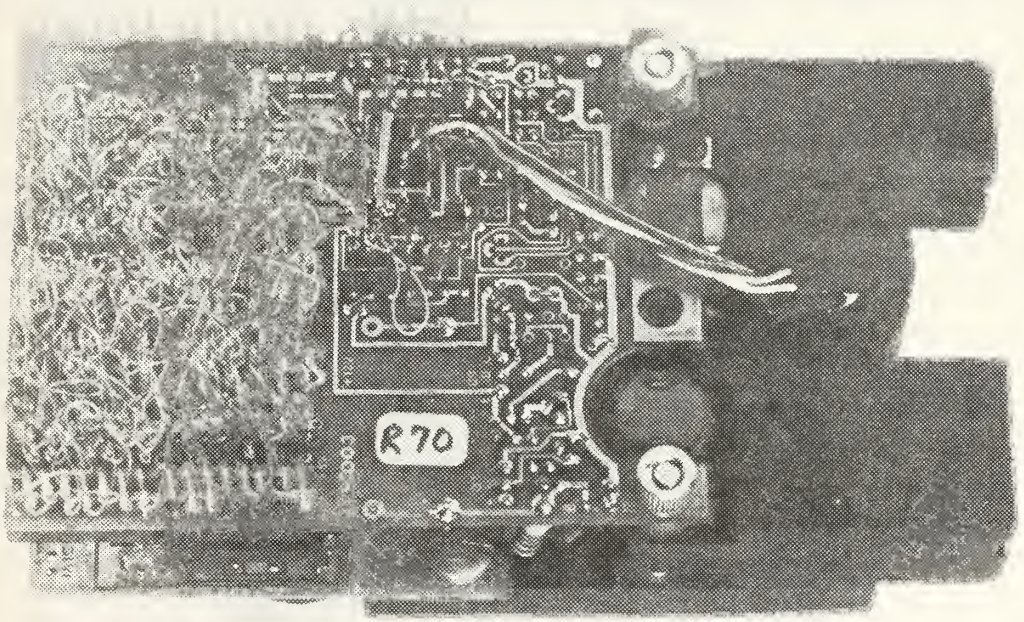

Figure II-3. Microvox Microrecorder

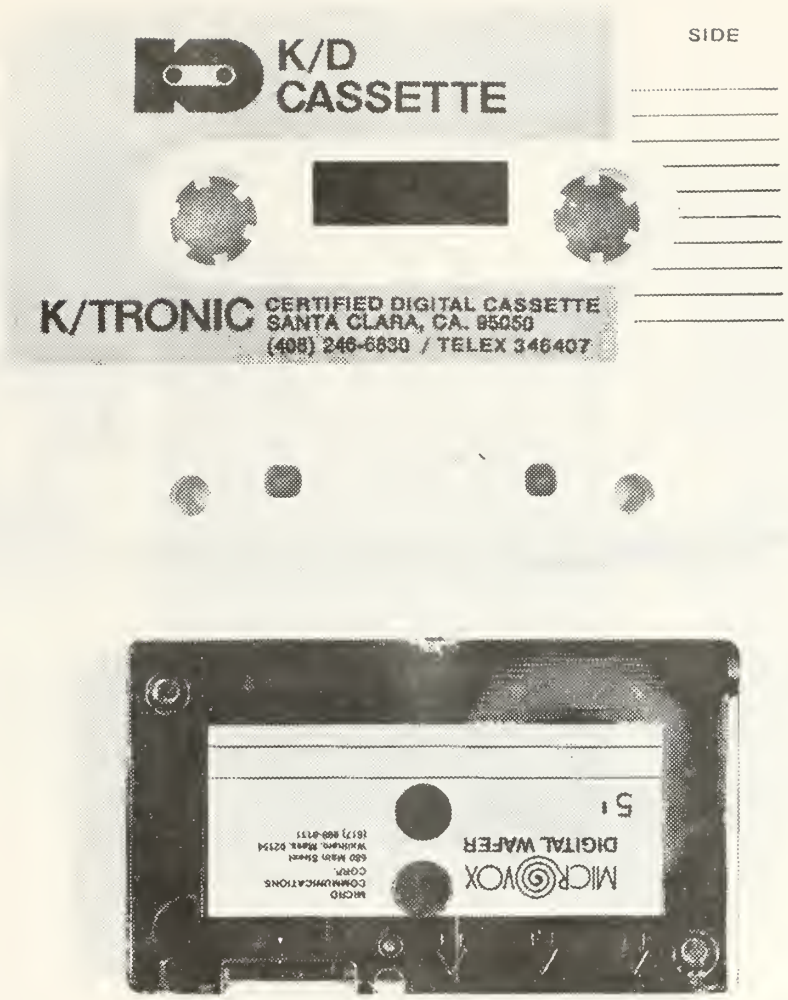

Figure II-4. Microvox Wafer and a Cassette

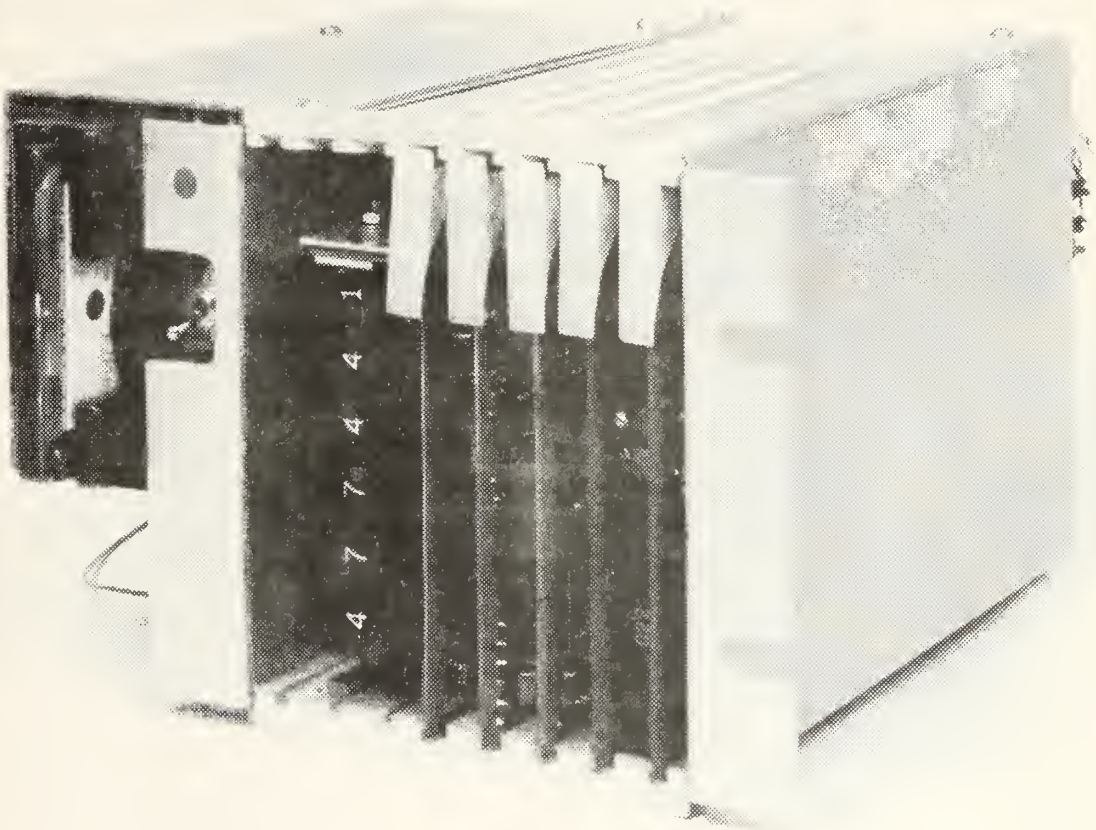

Figure II-3. Assembled Midas FLD System

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